AMENDMENTS TO THE SPECIFICATION

Applicant has reviewed the specification of the above referenced application, and herewith submits amendments to the specification to correct a few informalities. Amendments to the specification can be found below. Specifically, corrections have been made to page 6.

The specification is changed as follows:

Page 6, ln. 16, please correct the third paragraph, with the following correction:

As a correlator with a reduced circuit scale, there is proposed in our earlier patent application (JP Patent Application 11-265040, nor laid-open at the time of filing of the present Japanese application, now JP-A- 2001- 094468) ...

Please delete the present Abstract of the Disclosure and replace it with the following new Abstract of the Disclosure.

A fixed pattern detection device in which the device is fed as a received signal with a pattern of a length of N chips. The received signal is obtained by dividing and re-arraying each of K (integer) symbols in terms of a chip period as a unit, each symbol being spread with the spread code (PN) at a rate of M (integer) chips per symbol, and on repeatedly inserting into the re-arrayed symbols a signature pattern of a length K having one chip period as a unit, by M times, where N = K x M. The device includes first-stage correlators taking correlation between M received signals and M spread code sequences obtained on decimating a spread code sequence of a length N, and a second stage correlators taking correlation between the correlation values associated with K signatures output by the first-stage correlators and a pre-defined signature pattern.